

# METHOD OF INHIBITING METAL SILICIDE ENCROACHMENT IN A TRANSISTOR

## Related Application

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This application is related to my copending U.S. Patent Application Serial No. 10/718,892 entitled "Semiconductor Device With Silicided Source/Drains" and assigned to the assignee hereof.

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## Field of the Invention

This invention relates to semiconductor devices, and more particularly, to semiconductor devices with silicided source/drains.

## Related Art

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In common semiconductor manufacturing, semiconductor devices are made with lightly-doped drains at the junction with the channel and a relatively higher doped drain region used for making contact. The sources are made in the same way. The contact to the drain is made using a metal silicide. This contact is achieved by depositing the metal layer then reacting the metal layer with the silicon of the heavily-doped drain contact region to form a metal silicide contact region. The unreacted metal, which is located in the regions where there is no silicon, is then etched away with an etchant that is selective to the metal silicide. This metal silicide is then the contact point for the source and the drain of the semiconductor device.

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One effective metal has been found to be cobalt. Cobalt is effective but has been found to be difficult to use for very small polysilicon dimensions. Thus, with cobalt there have been problems with achieving reliable and continuous cobalt silicide formed on narrow polysilicon lines. This is even called the "line width effect." Thus, other metals have been studied to overcome this problem. One promising metal is nickel. The use of nickel to form nickel silicide is effective for narrower line widths than have been found to be achievable for cobalt silicide. A difficulty with nickel silicide, however, has been encroachment of the silicide phase under a transistor spacer and into the channel regions of a transistor. This encroachment leads to electrical short circuiting of elements of the transistor, such as short

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circuiting between the source, drain and well. The encroachment therefore leads to very low integrated circuit manufacturing yields. There is a need for a technique for forming nickel silicide on source/drains that has improved manufacturability for transistors in an integrated circuit.

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#### Brief Description of the Drawings

The present invention is illustrated by way of example and not limited by the accompanying figures, in which like references indicate similar elements, and in which:

10 FIGs. 1-4 are cross sections of a semiconductor device at sequential stages in processing according to an embodiment of the invention; and

FIG. 5 illustrates in flow chart form processing steps associated with a method for inhibiting metal silicide encroachment in a transistor.

15 Skilled artisans appreciate that elements in the figures are illustrated for simplicity and clarity and have not necessarily been drawn to scale. For example, the dimensions of some of the elements in the figures may be exaggerated relative to other elements to help improve the understanding of the embodiments of the present invention.

#### Detailed Description of the Drawings

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Illustrated in FIG. 1 is a semiconductor device 10 having a substrate 12 upon which there is formed an integrated circuit including a transistor. The semiconductor device 10 has a source 14, a drain 16 and a gate 22. It should be understood herein that the use of a source and drain may be reversed in the illustrated form of semiconductor device 10. The gate 22 is separated from the substrate 12 by a gate dielectric 20 that is one of numerous insulating materials used in semiconductors. Adjacent the gate 22 and overlying a portion of the source 14 and drain 16 is a sidewall dielectric 23. Adjacent the sidewall dielectric 23 is a sidewall spacer 24. Overlying these elements is a metal layer 25. In one form, the metal layer 25 is made of nickel (Ni), but other metals may be used. Metal layer 25 is a conformal layer. 25 Overlying metal layer 25 is a protection layer or cap layer 27. The cap layer 27 is typically a refractory metal or a refractory metal nitride such as Titanium (Ti) or Titanium Nitride (TiN). The cap layer 27 is also a conformal layer. Cap layer 27 functions to prevent exposure of the metal in metal layer 25 to a non-inert ambient between processing steps and therefore to

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prevent oxidation. It should be understood that the use of cap layer 27 is however optional. While a specific structure of semiconductor device 10 is illustrated, it should be understood that other transistor structures may be used in connection with the following processing steps to be described below. For example, a transistor having raised source and drain regions  
 5 overlying an upper surface of the substrate 12 may be used. Additionally, the substrate 12 may overlie an insulator (not shown) and function as a silicon-on-insulator (SOI) structure. Substrate 12 may be implemented using single crystal silicon, germanium doped single crystal silicon or other silicon based epitaxial layers having other dopant materials.

Illustrated in FIG. 2 is semiconductor device 10 upon further processing. In particular, a low temperature (i.e. temperatures for nickel silicide in a range of approximately  
 10 200 degrees Centigrade to 400 degrees Centigrade) anneal is implemented to form silicide regions 28, 29 and 30 respectively within the source, gate and drain. In one form when nickel is the metal, a thirty second anneal at a temperature of 340 degrees Centigrade is desirable.

A low temperature anneal is very important for the reason that when low temperature  
 15 is used, lateral encroachment of newly formed silicide regions is avoided. Lateral encroachment in this context is the creation of silicide in areas that are underneath the sidewall spacer 24 and underneath the gate 22 in the channel region (not numbered). This encroachment leads to electrical short circuiting of elements of the transistor, such as short circuiting between the source, drain and well. The encroachment therefore leads to very low  
 20 integrated circuit manufacturing yields. The encroachment is related to the high diffusivity of the metal coupled with the instability of the metal silicide phase. For example, under thermo-mechanical stress that exists in an integrated circuit, NiSi to NiSi<sub>2</sub> transformation takes place at moderately low temperatures just above 400 degrees Centigrade for nickel silicide. The formation of NiSi<sub>2</sub> consumes additional silicon and under the influence of the existing  
 25 thermo-mechanical stresses proceeds laterally, thereby resulting in encroachment in the transistor's channel region.

When nickel in metal layer 25 and silicon in source 14 and drain 16 are heated to form a silicide, various phases of a silicide are possible. That means, for example, that Ni<sub>2</sub>Si, Ni<sub>3</sub>Si and Ni<sub>31</sub>Si<sub>12</sub> may be present. As temperatures in the 200 hundred to 400 hundred  
 30 Centigrade range stated above increase, the higher temperatures will tend to make these phases convert to NiSi followed by conversion to a thermodynamically stable NiSi<sub>2</sub> phase which results in encroachment. Therefore, the higher temperatures in this range may not always result in optimal structures. In any event, a low temperature anneal for nickel that is

below 400 degrees Centigrade is desired. It should be understood that other temperature ranges exist when other types of metal silicide are used. For example, if cobalt silicide is used, a typical low temperature anneal range is approximately 400 degrees Centigrade to 550 degrees Centigrade. Within the area where source 14 was, there remains an unsilicided portion 15 immediately below silicide region 28 which now becomes the source of the semiconductor device 10. Silicide region 28 functions as an electrical contact to the unsilicided portion 15 functioning as the source. Within the area where drain 16 was, there remains an unsilicided portion 17 immediately below silicide region 30 which now becomes the drain of the semiconductor device 10. Silicide region 30 functions as an electrical contact to the unsilicided portion 17 functioning as the drain. The gate 22 is also modified. In particular, gate 22 is made smaller in total area by having a reduced height as a result of the formation of silicide region 29.

Illustrated in FIG. 3 is further processing of semiconductor device 10 wherein unsilicided portions of both the metal layer 25 and cap layer 27 are removed. The selective removal of these two layers is performed by an etch such as a conventional wet etch. The metal layer 25 functions to create the silicide regions 28, 29 and 30 in response to annealing. Once the silicide regions 28, 29 and 30 are formed, the unsilicided portions of metal layer 25 and its protective cap layer 27 (if implemented) are no longer needed. The wet etch chemistry leaves exposed surfaces of silicide regions 28, 29 and 30, sidewall spacer 24 and sidewall dielectric 23 without significantly modifying or damaging these surfaces.

Illustrated in FIG. 4 is a processing step that is performed after the selective removal of the unsilicided portions of metal layer 25. In FIG. 4 an ion implant 32 of an ion species is performed. The ion implant 32 is an implant of ions of specific composition. In one form, nitrogen ions [either N or N<sub>2</sub> (dinitrogen)] are implanted. In other forms, either a hydrogen ion implant or a fluorine-based ion implant is performed. The ions are driven into each of the silicide regions 28, 29 and 30. Some penetration into sidewall spacer 24 occurs, but will have no electrical impact. The dose and the energy of the implanted ions are chosen such that the implant penetrates the entire region of silicide regions 28 and 30. In other words, the implanted ions go through each of these two regions and can go as far as slightly below each of silicide regions 28 and 30. It is desired to set the dosage and energy level to values such that the implanted ions do not go much further than immediately below the lower surface of each of silicide regions 28 and 30. In order to attain the desired ion implant, nitrogen (N<sub>2</sub>) ions have an energy level that is approximately in the range of 1Kev to 10Kev. The value of

the energy level that is desired within this range depends upon, in part, the thickness of the silicide regions 28 and 30. These thicknesses are a function of how thick the original metal layer 25 was. For a 200 Angstrom thick nickel silicide region 28 and 30, a desirable energy level for an N<sub>2</sub> ion implant to use in the implant is 5KeV. It should be understood that other energy levels will be appropriate for other ion materials. In order to attain the desired ion implant, a dosage level for nitrogen (N<sub>2</sub>) ions approximately in the range of approximately  $1 \times 10^{14}$  to  $2 \times 10^{15}$  atoms per cm<sup>2</sup> is recommended. An optimum value of the dosage within this range may be found by experimentally implementing prototype samples over the stated range and measuring which ion dose results in least metal silicide encroachment while not otherwise affecting device electrical characteristics.

Upon completion of the implant, semiconductor device 10 of FIG. 4 is then exposed to a high temperature silicidation anneal. For this anneal, a high temperature is defined as being approximately equal to or above 400 degrees Centigrade when nickel silicide is utilized. For example, when a nickel silicide is implement a range of anneal temperatures in the range of approximately 400 degrees Centigrade to 450 degrees Centigrade is used for a thirty second period.

For other metal silicides, the values of the temperature ranges for the low temperature and the high temperature may vary. The high temperature anneal completes formation of silicide regions 28 and 30. Because the nitrogen ions are present in the silicide regions 28 and 30, no or minimal metal silicide encroachment into the channel region separating the source and drain is present.

Illustrated in FIG. 5 is a flowchart of a method of inhibiting metal silicide encroachment in a transistor. In a step 34, a transistor is formed. The transistor has two current electrodes, such as a source and a drain, and a control electrode such as a gate. The gate has a channel region separating the two current electrodes. The channel region is the area of the transistor in particular in which encroachment of metal silicide is desired to be prevented. In a step 36 a metal layer is deposited overlying the transistor. In one form, the metal is deposited by sputtering. The metal layer is conformal and numerous metals may be used. In particular, cobalt (Co) and nickel (Ni) are appropriate metals. In a step 38, a low temperature silicidation anneal is performed. In one form, this anneal is implemented as a conventional rapid thermal anneal (RTA). In another form, a low temperature anneal performed on a hot plate in an inert ambient is implemented. For embodiments using nickel, the anneal is substantially in a range of 200 degrees Centigrade to 400 degrees Centigrade.

By annealing at a temperature in this range, a metal silicide within the source and drain regions are formed without lateral growth of metal silicide towards the channel. In a step 40, unsilicided portions of the metal layer are selectively removed after the low temperature anneal. The selective removal is performed by a conventional wet etch. In a step 42, 5 encroachment inhibiting ions are implanted by using a predetermined dose and energy as described above. The order of the ion implant following a first or initial anneal to create silicide regions is important. By using a low enough temperature to avoid lateral metal silicide encroachment, a metal silicide region is created. When a subsequent implant of nitrogen ions is performed in step 42, the nitrogen ions will assist in inhibiting metal silicide 10 encroachment. In a step 44 a second anneal that is a high temperature anneal is performed. This anneal, in one form, is a rapid thermal anneal (RTA) that is conventional. In the presence of a metal silicide containing nitrogen ions, the nitrogen ions during this high temperature anneal substantially inhibit lateral metal silicide growth. It should be understood that step 44 is optional in the disclosed method at this point in time in those situations where 15 subsequent processing of the integrated circuit containing the device will experience thermal processing near the required temperature.

By now it should be appreciated that there has been provided a nitrogen implant into a metal silicide layer to retard metal diffusion and improve thermal stability. The implant energy and dose of the implant are optimized so that device performance is not affected and 20 the implant is restricted primarily to the metal silicide phase. Metal diffusion, such as in one form nickel diffusion, is retarded so that transformation of NiSi to NiSi<sub>2</sub> is delayed.

In the foregoing specification, the invention has been described with reference to specific embodiments. However, one of ordinary skill in the art appreciates that various modifications and changes can be made without departing from the scope of the present 25 invention as set forth in the claims below. For example, while a single transistor is illustrated, the inhibition of metal silicide encroachment as taught herein is particularly advantageous for a plurality of transistors that are co-proximately or closely located. Various types of transistors may be used with the method disclosed herein such as bipolar transistors that have base, collector and emitter terminals. The transistors may be configured in 30 numerous structural arrangements, such as being diode-connected where one of the current carrying electrodes is connected to a control electrode. Accordingly, the specification and figures are to be regarded in an illustrative rather than a restrictive sense, and all such modifications are intended to be included within the scope of present invention.

In one form there has been provided a method of inhibiting metal silicide encroachment in a transistor. A metal layer is deposited over a transistor structure. A silicidation anneal is performed to form metal silicide regions of terminals of the transistor structure at a first temperature sufficiently low to inhibit lateral encroachment of the metal silicide regions. Unsilicided portions of the metal layer are selectively removed from over the transistor. Encroachment inhibiting ions are implanted into the transistor after selectively removing the unsilicided portions of the metal layer. Another silicidation anneal is performed after implanting the encroachment inhibiting ions. In one form the step of performing another silicidation anneal after implanting the encroachment inhibiting ions is performed at a second temperature not substantially lower than the first temperature. In another form the first temperature is not substantially greater than 400°C. In this form the silicidation anneal after implanting the encroachment inhibiting ions is performed at a second temperature not substantially less than 400°C. In one form the metal that forms the metal layer is at least one of cobalt or nickel, and the metal silicide regions are a corresponding at least one of cobalt silicide or nickel silicide. In another form an encroachment inhibiting ion type is selected. An ion dose is determined before implanting the encroachment inhibiting ions. An ion energy is determined before implanting the encroachment inhibiting ions. In one form the encroachment inhibiting ions are selected from the group consisting of nitrogen-based ions, fluorine-based ions and hydrogen-based ions. In another form the encroachment inhibiting ions are dinitrogen. In one form the ion dose is determined to be less than  $2 \times 10^{15}$  ions/cm<sup>2</sup>. In another form the ion dose is determined to be greater than  $1 \times 10^{14}$  ions/cm<sup>2</sup>. In yet another form the ion dose is determined to be greater than  $1 \times 10^{15}$  ions/cm<sup>2</sup>. In yet another form the ion energy is determined to be less than 10keV. In another form the ion energy is determined to be greater than 1keV. In another form the ion energy is determined to be greater than 3keV. In one form the step of performing the silicidation anneal is the performance of a rapid thermal anneal.

In another form there is provided a method of improving thermal stability of a metal silicide to decrease encroachment on a transistor channel in a transistor. A metal layer over the transistor is deposited. A silicidation anneal is performed within a first temperature range to form metal silicide regions of transistor terminals of the transistor. Unsilicided portions of the metal layer are selectively removed from over the transistor. Encroachment inhibiting ions are implanted into the transistor terminals after selectively removing the unsilicided portions of the metal layer. A silicidation anneal is performed within a second temperature

range after implanting the encroachment inhibiting ions, the first temperature range including temperatures below temperatures in the second temperature range. In one form the first temperature range is selected to be sufficiently low to protect against lateral metal silicide mobility. In another form the second temperature range is selected to be sufficiently high to substantially complete metal silicidation. In one form the transistor terminals are a gate terminal and source/drain terminals. In another form the metal within the metal layer is nickel and the metal silicide regions are nickel silicide. In another form the encroachment inhibiting ions are dinitrogen gas ions. In another form a dinitrogen ion dose is selected having a value between  $1 \times 10^{14}$  and  $2 \times 10^{15}$  molecules/cm<sup>2</sup>. A dinitrogen energy is selected between 1keV and 10keV. In another form the dinitrogen ion dose is selected to be about  $5 \times 10^{14}$  ions/cm<sup>2</sup>. In another form the dinitrogen energy is selected to be about 5keV. A protection layer is formed over the metal layer after depositing the metal layer and before selectively removing the unsilicided portions of the metal layer. In one form the metal layer is nickel and the protection layer is titanium nitride. In yet another form there is provided a method of improving thermal stability of nickel silicide and inhibiting formation of nickel disilicide in a channel region of a transistor. A transistor structure including three transistor terminals is formed. Nickel is formed over each of the three transistor terminals. The transistor structure is heated at a temperature in a first temperature range sufficiently high to form nickel silicide regions of the three transistor terminals and sufficiently low to inhibit lateral encroachment of the nickel silicide regions. Encroachment inhibiting ions are implanted into the nickel silicide regions of the three transistor terminals after heating the transistor structure in the first temperature range. The transistor structure is heated at a temperature in a second temperature range after implanting the encroachment inhibiting ions. The first temperature range includes temperatures below temperatures in the second temperature range. The forming nickel over each of the three transistor terminals includes sputtering a layer of nickel over the transistor structure before heating the transistor structure. Unsilicided portions of the layer of nickel are wet etched from over non-terminal portions of the transistor structure after heating the transistor structure.

Benefits, other advantages, and solutions to problems have been described above with regard to specific embodiments. However, the benefits, advantages, solutions to problems, and any element(s) that may cause any benefit, advantage, or solution to occur or become more pronounced are not to be construed as a critical, required, or essential feature or element of any or all the claims. As used herein, the terms "comprises," "comprising," or any other



variation thereof, are intended to cover a non-exclusive inclusion, such that a process, method, article, or apparatus that comprises a list of elements does not include only those elements but may include other elements not expressly listed or inherent to such process, method, article, or apparatus.